K-BAND POWER GaAs FETs

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ABSTRACT

This paper will report on the structure and performance of GaAs FETs developed for K-band applications. A power output of 27dBm was obtained with 5dB gain at 21GHz.

A novel low loss waveguide to microstrip transition was used in the measurement. Its design will be described.

Introduction

Increased utilization of microwave communication systems has forced the use of higher frequency bands. Recently there has been considerable developmental activity at K-band frequencies. The most promising solid state devices for medium power amplification at these frequencies are GaAs FETs. This paper reports on the development of such GaAs FETs, with output powers in excess of 27dBm. The design incorporates features which give low thermal resistance, high efficiency, and reduced gate resistance.

Measurements of devices were performed in both a test fixture with conventional SMA connectors and in a low loss waveguide to microstrip transition fixture. The latter is capable of biasing the device with an external network.

Device Design

The approach in the design and fabrication of these K-band devices is similar to that reported earlier.[1] Devices are fabricated using a self-aligned gate process and are then flip-chip mounted into chip carriers. The starting point for the design of the K-band devices was the Ku-band devices previously described.[1] The Ku-band device is fabricated with a 1μm gate length and a 100μm gate width. The ultimate output power achievable by these devices in K-band can exceed the 0.4W/mm usually achieved by commercial devices, but it will be done at the expense of usable gain.

In order to improve the gain of a GaAs power FET, one would expect that the most significant factor is the reduction of gate length. This would reduce the gate to source capacitance and decrease the transit time. We have found that, in fact, the gain improvement due to gate length reduction alone is small. As the gate length is reduced below 1μm, fringing capacitive effects are significant. In addition, the parasitic gate resistance increases in direct proportion to the reduction in gate length. Computer modeling has shown that 1-2dB gain improvement can be achieved by reducing the parasitic gate resistance. This can be accomplished by reducing the resistance of each gate finger or by reducing the individual gate finger width while keeping the source periphery constant. The effect of the gate finger length reduction on the total parasitic gate resistance is shown in Figure (1). The curve has been normalized to a 150μm gate width device. The K-band devices have gate finger widths of 75μm, a reduction of 25% compared to the Ku-band device.

Self-aligned devices allow small source-gate and drain-gate spacing needed for low parasitic losses. This close gate-to-drain spacing was thought to cause low device breakdown voltages. However, it has been shown[2] recently that gate-drain avalanche breakdowns are not simply dependent on this spacing. The gate-drain avalanche breakdown limits the output power obtainable from a device. In fact, measured breakdowns of 20-25 volts are typical on the self-aligned devices that we fabricate. These devices have a gate-drain spacing of approximately one micron.

The limit of the power added efficiency is gate control of the device current. Because surface depletion is due to mid-gap pinning of the surface Fermi level[3], it is

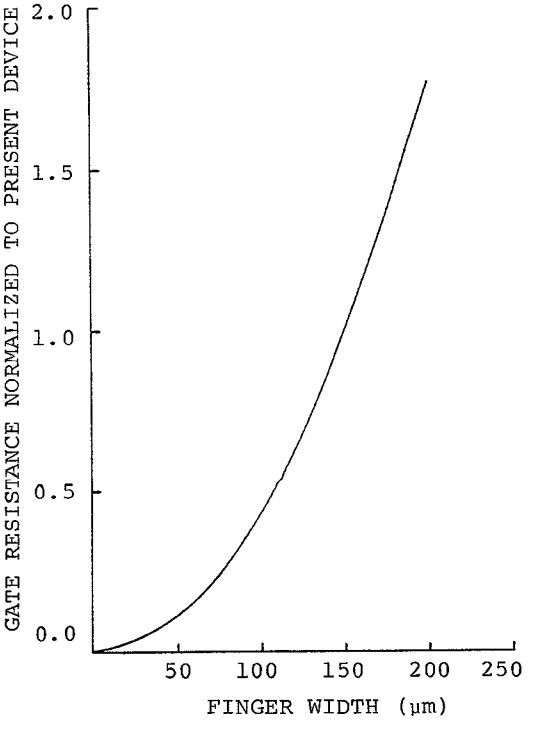

FIG. 1: EFFECT OF FINGER WIDTH ON GATE RESISTANCE FOR FIXED DEVICE SIZE.

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imperative to place the gate in a notch below the surface depletion. A novel self-aligned double recess has been achieved as is indicated in Figure (2). This allows for a gate recess below the surface depletion affording maximum control.

A completed device is shown in Figure (3). The very large source pads are for flip-chip mounting of the device. This allows for maximum heat sinking so that the thermal resistance for this 0.5 watt device is approximately 13°C/W compared to a C-band 0.5 watt device (MSC 88002), which is typically 25°C/W. Flip-chip mounting also insures a very low source inductance. This is particularly important at high frequencies for power combining and broadband matching.[1]

Novel Test Fixture

The most common mode of transmission at frequencies above 18GHz is waveguide. However, microstrip is the most convenient transmission line for solid state devices. A straightforward technique to couple waveguide to microstrip is to use waveguide to SMA and SMA to microstrip transitions. Commercial SMA to microstrip launchers can have losses as high as 1dB at 20GHz. A lower loss technique is direct waveguide to microstrip coupling. This is usually done by using a quarter wave ridge transformer mounted in the waveguide.[4,5] Utilization of such a structure requires DC bias and blocking on the microstrip circuit. The bias is supplied through a lowpass filter, based on lumped or distributed elements, and blocking is accomplished by a series capacitor or a coupler. The biasing and blocking elements add loss and increase the complexity of the microwave circuit.

We have developed a technique that uses the direct waveguide-microstrip transition for both RF and DC coupling. The schematic of this transition is shown in Figure (4). By DC isolating the ridge from the waveguide, the device can be biased without lumped or printed elements on the RF circuit. The bias network is completely external to both the waveguide and the microstrip. Figure (5) demonstrates a single stage K-band amplifier using this technique.

RF Results

Two devices were developed for use in K-band. The performance goals were power outputs of 24dBm and 27dBm, each with 4dB gain at 20GHz. To achieve the first goal, a 600µm source periphery device was designed incorporating the features discussed previously. At a drain voltage of 8.2V and 129mA drain current, an output power of 25dBm with 5dB gain at 20GHz was obtained. Under these conditions, the power added efficiency was 20%. The second device had a 1200µm source periphery. Its performance at 21GHz was 5dB gain with 27dB output power. The device was biased with a drain voltage of 9V and a drain current of 181mA. The power added efficiency realized was 21%.

Much of the recent interest in K-band applications is for space communications. This places a premium on device efficiency. Work[2] has been done indicating that thin

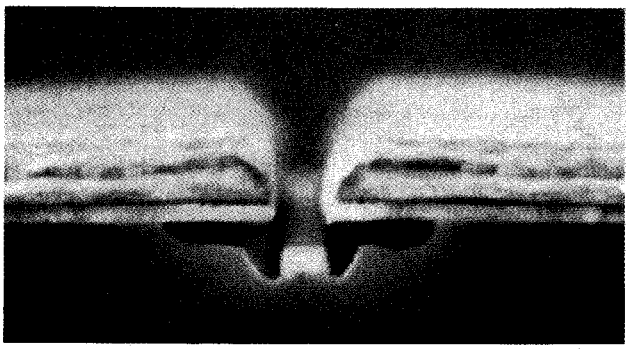

FIG. 2: SELF-ALIGNED DOUBLE RECESS

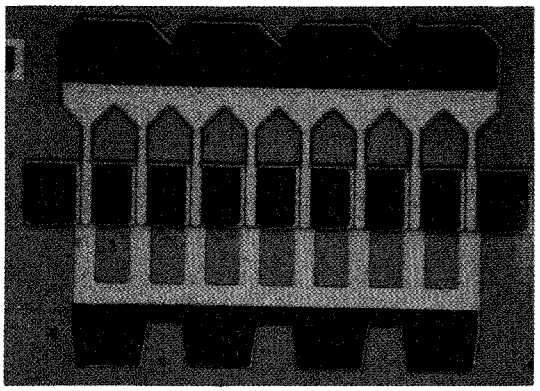

FIG. 3: 1200µm K-BAND POWER GaAs FET

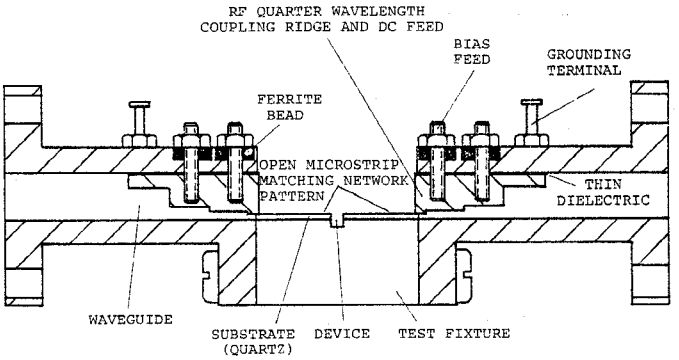

FIG. 4: A SCHEMATIC OF THE WAVEGUIDE TO MICROSTRIP TRANSITION WITH AN EXTERNAL BIAS.

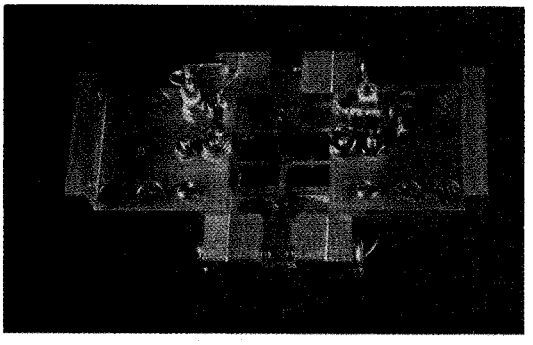

FIG. 5: K-BAND FET AMPLIFIER UTILIZING THE NOVEL APPROACH.

epitaxial material is necessary to achieve higher avalanche breakdown voltages. Additional work by the same group[3] relates the drain avalanche current to device power added efficiency. However, the avalanche mechanism limits the maximum power obtainable from the device and not the maximum power added efficiency. Figure (6) is the performance for a device at 22dBm input power

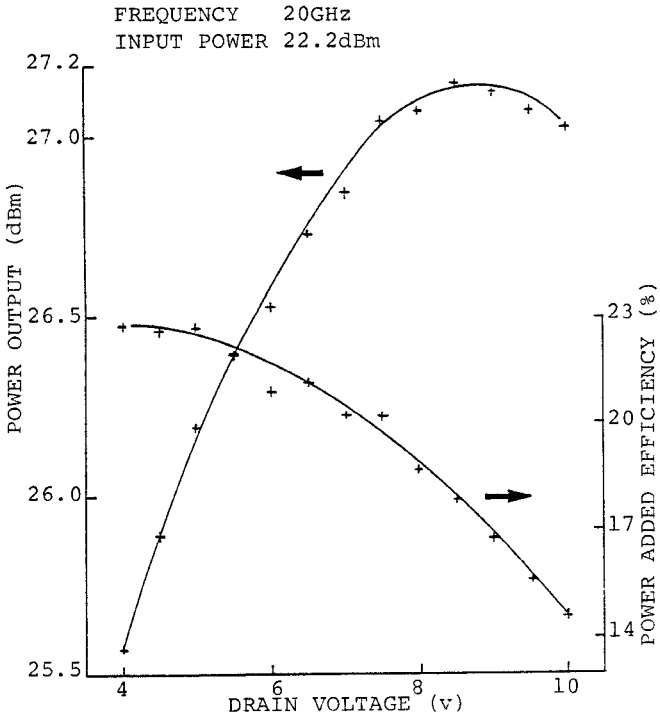

FIG. 6: OUTPUT POWER AND EFFICIENCY VERSUS DRAIN VOLTAGE.

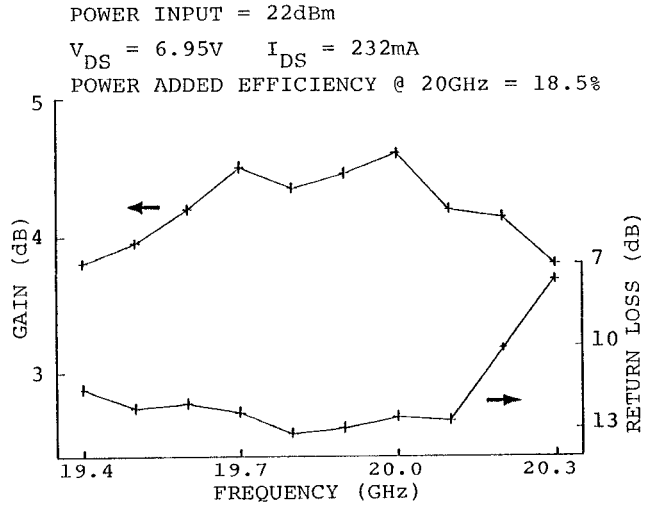

FIG. 7: GAIN AND RETURN LOSS OF A SINGLE STAGE AMPLIFIER.

operating at 20GHz. The output power and the power added efficiency are plotted versus the drain to source voltage. The power added efficiency is a maximum of 22.6%, at a drain-to-source voltage of 5V. The output power at this efficiency is only 26.2dBm while the maximum output power is 27.1dBm with an efficiency of 18%. The reason for this result is that the device bias can be adjusted to control the onset of avalanche. This can be used to trade output power for power added efficiency. It is significant to point out that for an output power of 27dBm, the power added efficiency is 20.4%.

The 1200μm device type was used for an amplifier at 20GHz. Results for the gain and return loss between 19.4 and 20.3GHz are shown in Figure (7). Connector and substrate losses were not taken into account in all of the above test conditions. Therefore the results due to the device itself can be somewhat better.

Conclusions

The structure of GaAs FETs has been described for K-band applications. A novel self-aligned double recess was developed that accounts for improved power added efficiency. A unique low loss waveguide to microstrip transition was developed that allows the bias circuitry to be external to both the waveguide and the open microstrip circuitry. RF data for a 600μm device and a 1200μm device at K-band was presented.

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